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INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(51) International Patent Classification 6 : G09G 3/36	A1	(11) International Publication Number: WO 99/38148
		(43) International Publication Date: 29 July 1999 (29.07.99)

(21) International Application Number: PCT/US99/01223

(22) International Filing Date: 22 January 1999 (22.01.99)

(30) Priority Data:
60/072,342 23 January 1998 (23.01.98) US

(81) Designated States: US, European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE).

Published
With international search report.
Before the expiration of the time limit for amending the claims and to be republished in the event of the receipt of amendments.

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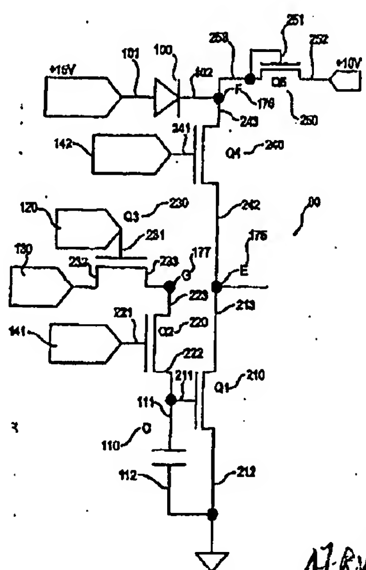
(54) Title: HIGH RESOLUTION ACTIVE MATRIX DISPLAY SYSTEM ON A CHIP WITH HIGH DUTY CYCLE FOR FULL BRIGHTNESS

(57) Abstract

An active matrix display device is disclosed. The display includes individual driver circuits for each pixel (100) to provide accurate, high resolution gray scale rendering and an almost 100 % duty cycle. The pixel circuit drivers (Figures 6(60) and 7(70)) minimize factors known to limit gray scale resolution, such as variations in threshold voltage, voltage drops in connecting lines and from leakage currents, and large peak currents. The present invention includes a line driver functioning initially as a low impedance voltage driver (Figure 6(60)), then converting to a high impedance current driver (Figure 7(70)). A method of driving a pixel (100) with sufficient circuitry to sustain the pixel's light output at a gray level determined by the input data fed to the pixel (100) is also disclosed. The display is capable of processing both digital and analog input data.



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HIGH RESOLUTION ACTIVE MATRIX DISPLAY SYSTEM ON A CHIP WITH HIGH DUTY CYCLE FOR FULL BRIGHTNESS

CROSS-REFERENCE TO RELATED PATENT APPLICATION

This application relates to and claims priority on provisional application serial number 60/072,342 filed January 23, 1998 and entitled "Active Matrix Display Using Individual Gray Scale Generator at Each Pixel Site."

FIELD OF THE INVENTION

The present invention relates to flat panel displays. In particular, the present invention relates to an active matrix display system on a semiconductor chip having a combination of a pixel cell and row/column driver that provide accurate, high resolution gray scale capability along with an almost 100% duty cycle for maximum light output.

BACKGROUND OF THE INVENTION

Today's software relies heavily on gray shades to provide high quality graphics and video in a wide variety of word processing, spreadsheets and other popular applications. A major factor in the overall quality of the displayed picture, color or monochrome, is gray level accuracy in the individual pixels over their entire dynamic range. Many flat panel light emitting devices fabricated on a chip operate with 256 levels of gray. In these devices the input brightness data are provided by eight digital bits (one byte).

In arrays with millions of pixels per display panel, it is almost impossible for the peripheral circuitry to sustain the high resolution data in every pixel, thus, compromises become necessary. For example, in an array of 1024x1024 pixel cells, the pixels in all the unselected 1023 rows are held in the "off" state while the peripheral circuit is processing, supplying, and sustaining the currents in the 1024 pixels of the selected row. With 1024 columns per row, a further compromise is often made by subdividing the columns into much smaller groups of 8, 16, 32 or 64 pixels per group. The groups are fed with current sequentially so that the demand on the peripheral circuitry is reduced to handling only 8 to 64 pixels at any time. A major disadvantage of this approach is that the active period of the pixels is reduced to a very small fraction of the frame period. To compensate for such a low duty cycle, the magnitude of the input current is increased by a correspondingly large number, if the pixel can tolerate it. However, the maximum current limit

of the pixel is often exceeded in the process and the net result is a significant reduction in the overall brightness level.

Ideally, the gray level subdivisions in a display are such that the brightness increments between the successive levels are uniform as perceived by the human eye and therefore, the ratio R of the pixel currents between any two adjacent gray levels is constant. For example, if the pixel current for the lowest gray level is 1 micro-amp (1 μA) and for the 256th gray level it is 100 μA, the value of the ratio R is approximately 1.0823. The current at the second gray level is therefore 1.0823 μA, at the third gray level it is 1.0823x1.0823 = 1.1714 μA and so on.

As shown in the above example, current increments between successive gray levels are very small. As a result, the combined effects of normal chip process tolerances, ambient temperature variations, power supply fluctuations, etc. may overwhelm the small increments and degrade the gray level accuracy.

Also, for moving pictures, the gray levels have to be changed at the frame rate, i.e., sixty times per second or faster. The circuit must therefore be capable of maintaining the integrity of the gray levels in an environment of high-speed switching. For displays using color, the time available is further reduced by one-third.

One method to overcome the limitations described above is to store the incoming brightness data sequentially in a set of input latches. After all the 1024 latches are loaded with the data, the row is selected to light up all the pixels simultaneously. However, this method also has disadvantages and limitations. For example, loading the incoming data in the latches takes considerable time, thus the duty cycle suffers. Also, simultaneous switching of all the 1024 pixels in the row induces large peak currents in the associated circuits and causes well-known simultaneous switching problems, including excessive voltage drops in the interconnecting lines and excessive induced noise.

There are a number of factors which limit a display panel's gray level resolution in typical integrated circuit environments. Applicants have designed an innovative circuit which minimizes the impact of these gray level resolution limiting factors, which are described in turn below.

1. <u>Variations in the Threshold Voltage Vt</u>

One factor which limits a display panel's gray scale resolution is variations in the threshold voltage. The light output of a pixel is exponentially dependent upon the input voltage, after subtracting the threshold voltage (Vt) from it. However, Vt of an individual pixel is unpredictable to a large extent because of the usual process tolerances and the local heat generated within the

immediate surrounding of the pixel. Ideally, the voltage fed to the pixel by the row/column driver should be automatically compensate for such changes.

2. Voltage Drops in the Connecting Lines

A second factor affecting gray level resolution is voltage drop. The gray level analog output voltage of a driver reaches a pixel after travelling through switching transistors and long, thin, sub-micron wide interconnecting lines, including the row/column lines. The total voltage drop in the connecting lines is therefore variable and another source of error.

The error is reduced if the pixel cell can be designed with at least one of its terminals connected directly to the relatively thick power supply or ground bus.

3. Voltage Drops Due to Leakage Currents

A third factor affecting gray level resolution is leakage currents. For 1024 rows and 1024 columns, a selected row line is connected to 1023 unselected columns and one selected column. Each column has at least one NFET (or PFET) terminal tied to every row line. If the NFET or PFET has, e.g., 1pA, of leakage current, the total leakage current fed to the row will be 1024 pA which may not be negligible. Also, the leakage currents are highly thermally sensitive and unpredictable.

4. Process and Power Supply Tolerances

A fourth factor affecting gray level resolution is process tolerances. The voltage generated by the D/A converter will be sensitive to the normal process tolerances and ambient temperature.

5. Large Peak Currents

A fifth factor affecting gray level resolution is large peak currents. Simultaneous switching of all the 1024 pixels in a row generates large peak currents in the associated circuits. The corresponding transient voltage changes in the power supplies can introduce significant error in the input data to the pixels. Simultaneous switching can also damage the pixels and even other parts of the chip.

For example, consider a P-channel transistor driving a pixel. Typically, its source is connected to the +5Volts power supply (Vdd) and its drain is connected to the anode of the pixel. Capacitor C may be tied across the source (Vdd) and the gate of the transistor in order to hold the gate at the desired voltage level. If the capacitor is charged to 4 Volts by the external circuit to feed a relatively large current (e.g. 10 micro-amps) into the pixel, the net gate voltage will be 5-4=+1 Volt.

In another situation, the Vdd supply may be pulled down to +4.5 Volts due to large peak currents at the time of charging the capacitor to 4 Volts. The gate voltage will now be 4.5-4=+0.5

Volt. After the switching transient has subsided and the Vdd supply settles back to +5 Volts, the gate voltage will pull back to less than +1 Volt due to parasitic capacitances associated with the gate. The actual gate voltage will lie somewhere between +1 Volt and +0.5 Volt, depending upon the ratio of capacitor C to the total parasitic capacitances. The net result is that the gate settles down to a voltage more negative than intended. With a P-type transistor, its output current increases exponentially as the gate becomes more negative, thus the current fed to the pixel will be much higher than intended. A similar situation may also arise with N-type transistors.

OBJECTS OF THE INVENTION

It is therefore an object of the present invention to provide a display panel which is less expensive to manufacture.

It is another object of the present invention to provide a display panel having simplified interfacing hardware to supply input data.

It is still another object of the present invention to minimize the complexity of the individual pixels in the display panel.

It is yet another object of the present invention to provide a more reliable display panel.

It is a further object of the present invention to provide a display panel with increased brightness.

It is still a further object of the present invention to provide a display panel having an increase in the duty cycle of the pixels to almost 100%.

It is yet a further object of the present invention to provide a display panel with circuitry that minimizes the peak currents of the pixel cells.

It is also an object of the present invention to increase the useful life of the pixel cells.

It is another object of the present invention to prevent premature burn-out of the pixel cells.

It is still another object of the present invention to provide a display panel with circuitry that reduces the errors arising from simultaneous switching of the row and column lines.

It is yet another object of the present invention to provide a display panel with circuitry that minimizes the problems arising due to voltage drops and induced noise.

It is a further object of the present invention provide a display panel with circuitry that eliminates simultaneous switching of a large number of pixel data.

It is still a further object of the present invention to provide a display panel with circuitry that reduces the errors associated with the use of current or voltage drivers for inputting data to the pixels.

It is yet a further object of the present invention to provide a display panel with circuitry that reduces the errors arising from variations in pixel threshold voltage.

It is also an object of the present invention to provide a display panel with circuitry that reduces the errors arising from leakage currents in the inactive devices in the unselected row and column lines.

It is another object of the present invention to provide a display panel with circuitry that reduces the effects of normal power supply tolerance and chip process tolerances.

It is yet another object of the present invention to provide a display panel with circuitry that allows input data to be fed at high speeds, to meet the requirements of high definition color panels with moving pictures.

It is still another object of the present invention to provide a display panel with pixel and interface circuits that consume low power and may be used in battery-operated applications.

Additional objects and advantages of the invention are set forth, in part, in the description which follows and, in part, will be apparent to one of ordinary skill in the art from the description and/or from the practice of the invention.

SUMMARY OF THE INVENTION

In response to the foregoing challenge, Applicants have developed an innovative, economical active matrix display device having a plurality of pixels arranged in a matrix. The display device may receive either digital or analog input data from a peripheral circuit.

The innovative display device of the present invention comprises means for directing the analog input data to a pixel driver circuit for at least one of the plurality of pixels; means for rapidly transmitting the analog input data, connected to the directing means; means for storing the analog input data, connected to the directing and transmitting means; means for drawing an analog current through a pixel, wherein the analog current corresponds to the analog input data and the drawing means are connected to the storage means, and whereby the pixel emits light output of intensity proportional to the analog current.

When digital input data are supplied to the display device, the device may further comprise means for converting the digital input data to analog input data. The converting means further

comprises at least one digital-to-analog converter which may be connected to the peripheral circuit and to the directing means.

The directing means of the display device further comprises at least one column line and at least one row line.

The transmitting means of the display device further comprises a line driver which may function initially as a low impedance voltage driver to charge up a data line to a new input voltage, then may automatically convert to a high impedance current driver.

The storage means of the display device further comprises a capacitor having a first end and a second end.

The drawing means of the display device further comprises a transistor connected to a strobing control line. The transistor may simultaneously activate the plurality of pixels.

An innovative method of driving a pixel in an active matrix display is also disclosed. The method comprises the steps of supplying either digital or analog input data from a peripheral circuit; directing the analog input data to a pixel driver circuit for a pixel; transmitting the analog input data rapidly; storing the analog input data; drawing an analog current through the pixel, wherein the analog current corresponds to the analog input data, and whereby the pixel emits light output of intensity proportional to the analog current.

When digital input data are supplied to the display device, the method of driving a pixel further comprises the step of converting the digital input data to analog input data.

The method of driving a pixel may further comprise the steps of using a linearizing impedance to enhance the gray level rendering accuracy of the light output of the pixel and adjusting the input data to compensate for ambient temperature, pixel threshold voltage and transistor threshold voltage.

The step of rapidly transmitting the analog input data may further comprise providing a line driver that functions initially as a low impedance voltage driver to charge up a data line to a new input voltage, then automatically converts to a high impedance current driver.

BRIEF DESCRIPTION OF THE DRAWINGS

The present invention will now be described in connection with the following figures in which like reference numbers refer to like elements and wherein:

Fig. 1 is a schematic diagram of a pixel driver circuit with a linearizing resistor according to an embodiment of the present invention.

Fig. 2 is a schematic diagram of a pixel circuit driver for pulse modulation according to an alternate embodiment of the present invention.

Fig. 2a is a graph depicting ramp voltage as a wave form.

Fig. 3 is a schematic diagram of a pixel driver circuit suitable for analog input according to an alternate embodiment of the present invention.

Fig. 4 is a schematic diagram of a known digital-to-analog converter with voltage output suitable for voltage-driven pixel cells of the present invention.

Fig. 5 is a schematic diagram of a known digital-to-analog converter with current output suitable for current-driven pixel cells of the present invention.

Fig. 6 is a schematic diagram of a pixel driver circuit with combined current and voltage drivers suitable for analog input according to an alternate embodiment of the present invention.

Fig. 7 is a schematic diagram of a voltage driver circuit according to an alternate embodiment of the present invention.

Fig. 8 is a schematic diagram of a pixel driver circuit suitable for analog input according to a preferred embodiment of the present invention.

DETAILED DESCRIPTION OF THE INVENTION

Reference will now be made in detail to embodiments of the present invention, examples of which are given in the accompanying circuit diagrams.

The following abbreviations and definitions apply throughout the following description of the present invention. N-channel Field Effect Transistor : N-FET; P-channel Field Effect Transistor : P-FET. A voltage level of +5 Volts is assumed for the logic "1" and 0 Volts is assumed for the logic "0". The voltage level could also be 3.3 Volts and 0 Volts, or any other reasonable set of voltages. A node is "up" if it is at +5Volts and "down" if it is at 0 Volts. A standard 5 Volts (or 3.3 Volts) CMOS process is assumed to be used in the fabrication of the chip for the present invention. It is further assumed that the junction breakdown voltage in the silicon is at least 10.7 Volts. Voltage may be readjusted if a junction breakdown is different from 10.7 Volts. The display panel circuitry of the present invention is sub-divided into the following sub-circuits: Pixel Cell; Pixel Circuit; Digital-to-Analog (D/A) Circuit; and Row and Column Drivers.

1. Pixel Cell

For the purposes of describing the present invention, it is assumed that the light-emitting pixel, abbreviated as Px or Px1, is processed after the silicon chip containing all the other circuit elements has been manufactured using a standard CMOS (Complimentary Metal Oxide Semiconductor) process. The pixel may consist of two or more transparent (or semi-transparent) organic layers which form the anode, the cathode and power supply electrodes of the pixel.

The following electrical characteristics of the pixel cell are assumed: maximum voltage is 15 Volts; threshold voltage is 4.3 Volts; and operating current range is 0 to 10 micro-amps. The actual values of these parameters may be different, based on the process used in the organic layers. The circuits described here will still be applicable but the component values may be readjusted accordingly.

2. Pixel Circuit

Pixel cell circuits are of two basic types, voltage-driven or current-driven. A voltage-driven pixel receives its brightness input data from the peripheral circuit in the form of an analog voltage, whereas a current-driven pixel receives its brightness input data from the peripheral circuit in the form of an analog current.

In a pixel containing a data storage capacitor, input data may be used for charging up the capacitor to an analog voltage level appropriate for the corresponding gray level output from the pixel. The charge on the capacitor may be used for sustaining a steady and continuous light output at that level even after the peripheral circuit is disconnected from the pixel. Alternately, the charge on the capacitor may be used to control the number of input pulses fed to the pixel to obtain the desired total light output from it.

Because of the exponential nature of the pixel's light output and its critical dependence upon the threshold voltage, compensation for variations in the threshold voltage can significantly improve the gray level accuracy.

a. Voltage-Driven Pixel Cell Circuit

Referring now to Fig. 1, a simple voltage-driven pixel cell circuit is shown as 10. Analog input data are fed to capacitor C 110 using conventional column select transistor Q1 210 and row select transistor Q2 220. The capacitor voltage is applied to gate 231 of third device Q3 230 whose drain 233 is connected to a suitable positive voltage +V while source 232 is connected to anode 101 of pixel 100. Cathode 102 of pixel 100 is grounded through resistor R 310 which helps to linearize pixel 100 light output vs. input voltage characteristics. The input voltage can therefore be made directly proportional to the desired light output after compensating for the

threshold voltage drops in pixel 100 and Q3 230 by the addition of a fixed voltage to the analog input. Errors due to threshold voltage drops in Q1 210 and Q2 220 can be almost eliminated by changing Q1 210 and Q2 220 to P-type devices and making the minimum input voltage more positive than the threshold voltages of Q1 210 and Q2 220. The polarity of the gate voltages will be reversed for the P-devices.

Resistor R 310 may be omitted (shorted out) by proper pre-compensation of the input data to account not only for the threshold voltage drops but also for the non-linear characteristics of the pixel.

Circuit 10 may be modified for use as a pulse modulated pixel circuit. Referring now to Fig. 2, pulse modulated pixel circuit 20 is shown. In Circuit 20, input data are received as a series of discrete narrow pulses applied to the "Ramp" terminal 140. Each successive pulse adds extra charge to capacitor C 110. The final voltage of capacitor C 110 therefore depends upon the number of input pulses; the pixel brightness varies accordingly. The effects of threshold drops in pixel 100 and Q3 230 must be pre-compensated by the peripheral circuitry to obtain high gray level resolution.

Alternately, instead of discrete pulses, capacitor C 110 may be charged up to the desired voltage level by an analog voltage applied to "Data" terminal 150 when both the "Row" 120 and "Column" 130 are selected. When all the pixels in the row are fed with new data in this manner, "Ramp" terminal 140 is supplied with the ramp waveform shown in Fig. 2a. The voltage on the "Ramp" line is normally held at 0V and is raised linearly to a suitable higher voltage e.g., +4V, for a given time before being brought down quickly to 0V again. After a brief pause, the cycle is repeated. The frequency of the ramp voltage depends upon the input data rate. The shape of the ramp voltage may be optimized for a given application, based on the device and pixel characteristics.

Assuming that the threshold voltages of Q3 230 and pixel 100 add up to 4V, circuit 20 operates as follows: when input data on column line 130 equal 0V, capacitor C 110 is charged to 0V by the input data. As the ramp voltage rises, the gate voltage of Q3 230 rises with it, while the voltage across capacitor C 110 remains nearly constant at 0V. The peak voltage on the gate 231 of Q3 230 is +4V and there is no current flow in pixel 100 because the sum of the threshold voltages of Q3 230 and pixel 100 has not been exceeded.

When input data on column line 130 equal +4V, the initial voltage on gate 231 of Q3 230 is +4V, and the ramp voltage is still at 0V. The gate voltage starts to rise with the ramp voltage and peaks at +8V when the ramp voltage reaches +4V. Pixel 100 is therefore turned on at the start

of the ramp and its current increases exponentially to the peak value corresponding to +8V on gate 231 of Q3 230. The total light output from pixel 100 is therefore very high. The pixel light output thus varies from zero to a high value, based on the analog input voltage fed to capacitor C 110 by "Data" terminal 150. Overall linearity between the digital input data and the pixel's gray level output can be maintained by tailoring the shape of the ramp voltage waveform to make it the inverse of the exponential shape of the pixel's output. Another option for both the ramp and the pulse inputs is to pre-compensate the digital input by using a look-up table, stored in a read-only memory as a part of the peripheral circuitry, to convert the incoming digital input into a compensated output for pixel 100.

Alternate methods for partial or full compensation include various types of circuits which can automatically adjust the pulse width and pulse amplitude, based on the input digital data, to obtain greater flexibility in controlling all the three attributes of the pulse train, namely, width, amplitude and the number of pulses. Although the peripheral circuit complexity increases considerably with the use of these types of circuits, it provides much better gray scale accuracy without making the pixel cell more complex. In some cases, with pre-compensation, the digital method can provide more precise gray level control than the analog method.

b. <u>Current-Driven Pixel Circuit</u>

Current-driven pixel cell circuit is shown in Fig. 3 as 30. Referring now to Fig. 3, anode 101 of pixel 100 is tied to the +15V supply and cathode 102 is tied to drain 243 of device Q4 240. Device Q4 240 is preferably on N-FET. Gate 241 of Q4 240 is tied to "-Row" control line 142. Source 242 Q4 240 is tied to drain 213 of device Q1 210. Device Q1 210 is preferably an N-FET. Source 212 of Q1 210 is grounded and gate 211 of Q1 210 is tied to first end 111 of capacitor C 110. Second end 112 of capacitor C 110 is also grounded. Source 222 of device Q2 220 is also tied to gate 211 of Q1 210, gate 221 of Q2 220 is tied to external control line "Str" 141 and drain 223 of Q2 220 is tied to drain 213 of Q1 210 as well as to drain 233 of device Q3 230. Gate 231 of Q3 230 is tied to control line "Row" and its source 232 is tied to 30 column line "Col" 130. Devices Q2 222 and Q3 230 are preferably N-FETs.

Circuit 30 operates as follows: initially, Q4 240 is switched off by bringing down "-Row" line 142. Simultaneously, row line 120 goes up to turn on Q3 230 so that the input analog current supplied by the column line 130 flows through Q3 230, thus raising the voltage on the node connective drains 333, 223 and 213. Control line "Str" 141 is also up at this time so that Q2 220 is conducting and the voltage on the node connecting drains 233, 223 and 213 charges up

capacitor C 110 which then turns on Q1 210 so that all the input current passes through Q1 210 to ground and an equilibrium is reached.

Next, control line "St" 141 is brought down to turn off Q2 220, thereby isolating capacitor C 110 from the external lines. The charge on capacitor C 110, however, remains unaffected.

Finally, row line 120 is brought down to turn off Q3 230 and simultaneously "-Row" line 142 goes up to turn on Q4 240. The current flowing through Q1 210 is now fed to pixel 100 through Q4 240.

The threshold voltages of the devices do not impact the current fed to pixel 100 and the gray level accuracy is therefore well maintained. In practice, however, the inter-electrode capacitances of the devices and their leakage currents do affect the pixel current unless the storage capacitor is big enough to make the resulting error negligible.

3. Digital-to-Analog Circuit

Digital-to-Analog converter 40 (D/A converter) with voltage output is shown in Fig. 4. The eight digital input data lines are connected to the gates of eight transistors, their sources are tied to ground through series resistors with values ranging from R/16 to 8R, where R is a resistor value consistent with the circuit requirements. In D/A converter 40, the total current flows through resistor R1 so that the voltage available at the output terminal (source) of the output device 41 is the analog equivalent of the digital input except for the voltage drop due to the threshold voltage of device 41 which needs to be compensated for.

Digital-to-Analog converter 50 with current output is shown in Fig. 5. In D/A converter 50, the total current flows through a P-device 51 and the output current available at the output terminal (drain of device 52) is the analog equivalent to the digital input by the "current mirror" action between devices 51 and 52.

4. Row and Column Driver Circuits

Applicants have designed an innovative "line driver" circuit which combines the attributes of a voltage driver and a current driver to provide fast and accurate delivery of the analog output of a D/A converter to the pixel cells. The following description of a "line driver" is equally applicable to both a row driver and a column driver.

The D/A converter provides an accurate analog output at its output terminal. However, since the D/A converter is located on the chip along the periphery of the pixel array, the D/A output has to pass through relatively long and thin row/column lines and several active devices to reach pixel 100.

Because a voltage line driver has low output impedance, it may charge up the line relatively quickly, but there will be voltage drops in the devices and the interconnecting long lines so that some of the output voltage will be lost in transit, resulting in significant error in the pixel output. Thus, high speed is gained at the cost of gray level error.

If a current driver is used, however, the current reaching pixel 100 at the end of the interconnecting lines will be the same as the output current of the D/A converter (except for leakages and transient capacitance charge up currents which are ignored here). Current drivers have very high output impedance, increasing the time taken to charge up the line to the final value. Thus, gray level accuracy is gained at the cost of speed.

Applicants' innovative driver acts as a voltage driver initially, with low output impedance, to charge up the line quickly to nearly the final voltage level, so speed is gained. Then the circuit automatically converts itself into a current driver to ensure that the current at the pixel end is the same as the D/A output current, so accuracy is gained. Applicants' design thus supplies the best of both types of drivers without the drawbacks of either.

Referring now to Fig. 6, a combined current and voltage driven circuit is shown as 60. D/A converter 50 (current output type) is modified to obtain two identical output current sources, first output current source J1 161 and second output current source, J2 162, by adding an extra P-FET device (not shown in Fig. 5) in parallel with device 52. The output of second current source J2 162 is fed to gate 211 and drain 213 of a local N-FET device Q1 210. Q1 210 corresponds to device Q1 210 of Fig. 3. Drain 212 of local device Q1 210 is grounded. Since the Q1 210 devices of Figs. 3 and 6 are identical, the voltage developed at gate 211 of Q1 210 of Fig. 6 is such that, if applied to gate 211 of Q1 210 of Fig. 3, the current in drain 212 of Q1 210 of Fig. 6 will be equal to the current in second output current source J2 162.

With continued reference to Fig. 6, the output of first output current source J1 161 is tied to gate 231 of device Q3 230 and it is also tied to column line 130 of Fig. 3 to provide accurate current input to pixel 100, even though it will be a slow process. Devices Q2 220 and Q3 230 form a differential amplifier, with Q5 250 as its current source. The magnitude of the current is controlled by resistor R1 310 and device Q4 240. Drain 223 of Q2 220 is tied to the +5V supply through load resistor R2 320. Drain 233 of Q3 230 is also tied to the +5V supply through second load resistor R3 330, which is identical to first load resistor R2 320.

If at any given time the voltage developed at drain 213 of Q1 210 is higher than the voltage at gate 231 of Q3 230, the voltage at output node "A" 171 will be lower than the voltage at output node "B" 172 and vice-versa. This results in an output differential voltage "Vdiff" across the

nodes "A" 171 and "B" 172, which is fed as input to a voltage driver described in connection with Fig. 7, below.

Referring now to Fig. 7, a voltage driver is shown as 70. Vdiff of Fig. 6 is applied to the input node "A" 173 and input node "B" 174 of voltage driver 70 which pulls column line 130 up or down to reduce the magnitude of Vdiff. When Vdiff falls below 0.7 V (threshold voltage), voltage driver 70 is automatically deactivated. Voltage driver 70 comprises: N-FET device Q5 250 with source 252 connected to input node "A" 173, gate 251 connected to input node "B" 174 and drain 253 to gate 271 of P-FET device Q7 270. Input node "A" 173 is also connected to source 262 of a P-FET device Q6 260, whose gate 261 is tied to input node "B" 174 and whose drain 263 is tied to gate 281 of N-FET device Q8 280. Source 282 of Q8 280 is grounded and its drain 283 is connected to column line 130. Gate 281 of Q8 280 is also grounded via resistor R5 350. Source 272 of Q7 270 is tied to the +5V supply and its drain 273 is tied to column line 130. Gate 271 of Q7 270 is tied to the +5V supply through resistor R4 340. In some cases, it may be desirable to replace the two resistors with small current sources.

Voltage driver 70 operates as follows: if Vdiff is greater than a threshold voltage (assumed to be 0.7Volts hereafter), with input node "A" 173 more positive than input node "B" 174, the P-FET device Q6 260 conducts. The voltage on gate 281 of Q8 280 rises to the voltage level of input node "A" 173 and device Q8 280 therefore conducts to lower the voltage of column line 130. Because Q5 250 is off, Q7 270 is also off during this time. As a result of bringing down the voltage of column line 130, Vdiff falls below 0.7 Volts, thereby turning off both Q6 260 and Q8 280. Q5 250 and Q7 270 continue to remain off so that all the devices are off and the driver is completely off with high output impedance at column line 130.

Similarly, if input node "B" 174 is more positive than input node "A" 176, Q6 260 and Q8 280 continue to remain off whereas Q5 250 and Q7 270 are turned on to raise the voltage on column line 130. This again reduces Vdiff to below 0.7 Volts, after which Q5 250 and Q7 270 also turn off.

The Preferred Embodiment

Referring now to Fig. 8, a preferred embodiment of the present invention is shown as circuit 80. As embodied herein, anode 101 of pixel 100 is tied to the +15Volts power supply whereas cathode 102 is tied to drain 243 of N-FET device Q4 240. Gate 241 of Q4 240 is tied to external control line "-Row" 142. Source 242 of Q4 240 is tied to drain 213 of N-FET Q1 210 at node E 175. Gate 211 of Q1 210 is tied to first end 111 of storage capacitor C 110. Source 212 of Q1 210 is grounded. Second end 112 of capacitor C 110 is also grounded. A third N-FET Q2

220 has its drain 223 connected to drain 213 of Q1 210. Gate 221 of Q2 220 is tied to external strobing control line "Str" 141. Source 222 of Q2 220 is tied to gate 211 of Q1 210. N-FET Q3 230 has its drain 233 tied to drains 213 and 223 of Q1 210 and Q2 220. Gate 231 of Q3 230 is tied to row line 120. Source 232 of Q3 230 is tied to column line 130. A fifth N-FET Q5 250 has its gate 251 and drain 253 tied to cathode 102 of pixel 100. Source 252 of Q5 250 is tied to an external +10Volts power supply.

Circuit 80 operates as follows: When transistors Q4 240 and Q5 250 are off pixel, current is zero and pixel 100 is turned off. Cathode 102 of pixel 100 will therefore tend to rise to +15Volts to reduce the voltage difference between the anode and cathode to zero, the normal condition for turning off a pixel. Because cathode 102 of pixel 100 is tied to drain 253 of transistor Q5 250 and also to drain 243 of Q4 240, the drain voltages will also rise to +15Volts, which exceeds the breakdown limit of 10.7 Volts in the silicon chip. Such a high voltage is unacceptable, thus transistor Q5 250 has been added to the circuit. Assuming that the threshold voltage of Q5 250 is 0.7 Volts, Q5 250 will turn on soon as the voltage at node F 176 exceeds 10.7 Volts, thus preventing cathode 102 of pixel 100 from going more positive. The minimum pixel voltage, therefore, will be 4.3 Volts (not zero volts) which is acceptable if the pixel threshold voltage is greater than 4.3 Volts. If not, the voltage levels will have to be readjusted. With continuing reference to Fig. 8, pixel 100 may also be turned on. Initially, row line 120 is up so that Q3 230 is on its complement line "-Row" 142 is down so that Q4 240 is off. Strobing control line "Str" 141 is up so that Q2 220 is on. Also, column line 130 is primed by the associated pixel driver to supply the desired current from the pixel e.g., 1 micro-amp. As column line 130 pushes its current into the node G 177 via device Q3 230, the voltage there rises (goes more positive) and because Q2 220 is on, the current starts to charge up capacitor C 110. This makes gate 211 of Q1 210 increasingly positive so that Q1 210 starts to draw current. Soon an equilibrium is reached such that the charge on capacitor C 110 and the voltage on gate 211 of Q1 210 draw all the current supplied by column line 130. After sufficient time for the equilibrium to be reached, Q2 220 may be turned off by bringing down strobing control line "Str" 141. Thus, the input data are strobed and used to charge up gate 211 of Q1 210 to the correct level to draw 1 micro-amp current.

Next, strobing control line "Str" 141 is brought down to turn off Q2 220 and isolate capacitor C 110 from node G 177. Transistor Q1 210 continues to draw 1 micro-amp from column line 130 through Q3 230.

Finally, row line 120 is brought down and its complement, control line "-Row" 142, is brought up. The current drawn by Q1 210 is now diverted from column line 130 to pixel 100.

through transistor Q4 240. Pixel 100 continues to remain lit with 1 micro-amp current, irrespective of the condition of column line 130, which may change its current level to some other value for feeding the next pixel in the row.

As embodied herein, first row line 120 and first column line 130 are selected and condition the associated pixel driver 80 to deliver the current for the first pixel to the column line 130. Strobing control line "Str" 141 is turned on when column line 130 is ready with the data and capacitor C 110 is charged up to the correct level by the input current. Next, strobinhg control line "Str" 141 is brought down to free column line 130 for serving the next pixel in the row. Pixel 100 continues to be lit with the current fed to it.

The process is repeated to cover all the pixels in the row, after which the process is repeated by selecting the next row and so on until all the pixels in the panel are lit with the correct input currents. When data arrive for the next frame, the whole process is repeated. This completes the operating sequence of circuit 80 of the present invention.

Pixel 100 is current driven, thus the input data to pixel 100 are supplied in the form of an analog current, not voltage.

It will be apparent to those skilled in the art that various modifications and variations can be made in the construction and configuration of the present invention without departing from the scope or spirit of the invention.

For example, other types of active devices may be used in the circuits of the present invention, resulting in similar circuits with different combinations of - and P-type Field Effect Transistors, junction gate and bipolar transistors.

Thus, it is intended that the present invention cover the modifications and variations of the invention.

What is claimed is:

1. An active matrix display device having a plurality of pixels arranged in a matrix, said device being capable of receiving at least one of digital and analog input data from a peripheral circuit, comprising:

means for directing said analog input data to a pixel driver circuit for at least one of said plurality of pixels;

means for rapidly transmitting said analog input data, connected to said directing means;

means for storing said analog input data, connected to said directing and transmitting means;

means for drawing an analog current through said at least one pixel, wherein said analog current corresponds to said analog input data and said drawing means is connected to said storage means, and whereby said at least one pixel emits light output of intensity proportional to said analog current.

2. The device of Claim 1, further comprising means for converting said digital input data to analog input data, connected to said peripheral circuit and to said directing means.

3. The device of Claim 2, wherein said converting means further comprises at least one digital-to-analog converter.

4. The device of Claim 1, wherein said directing means further comprises at least one column line and at least one row line.

5. The device of Claim 1, wherein said transmitting means further comprises a line driver functioning initially as a low impedance voltage driver to charge up a data line to a new input voltage, then automatically converting to a high impedance current driver.

6. The device of Claim 1, wherein said storage means further comprises a capacitor having a first end and a second end.

7. The device of Claim 1, wherein said drawing means further comprises a transistor connected to a strobing control line.

8. The device of Claim 7, wherein said transistor simultaneously activates said plurality of pixels.

9. A method of driving a pixel in an active matrix display, comprising the steps of:

supplying at least one of digital and analog input data from a peripheral circuit;

directing said analog input data to a pixel driver circuit for said pixel;

transmitting said analog input data rapidly;

storing said analog input data;

drawing an analog current through said pixel, wherein said analog current corresponds to said analog input data, and whereby said pixel emits light of intensity proportional to said analog current.

10. The method of claim 9, further comprising the step of converting said digital input data to analog input data.

11. The method of claim 9, further comprising the step of using a linearizing impedance to enhance the gray level rendering accuracy of said light output of said pixel.

12. The method of claim 9, further comprising the step of adjusting said input data to compensate for ambient temperature, pixel threshold voltage and transistor threshold voltage.

13. The method of claim 9, wherein the step of rapidly transmitting said analog input data further comprises providing a line driver that functions initially as a low impedance voltage driver to charge up a data line to a new input voltage, then automatically converts to a high impedance current driver.

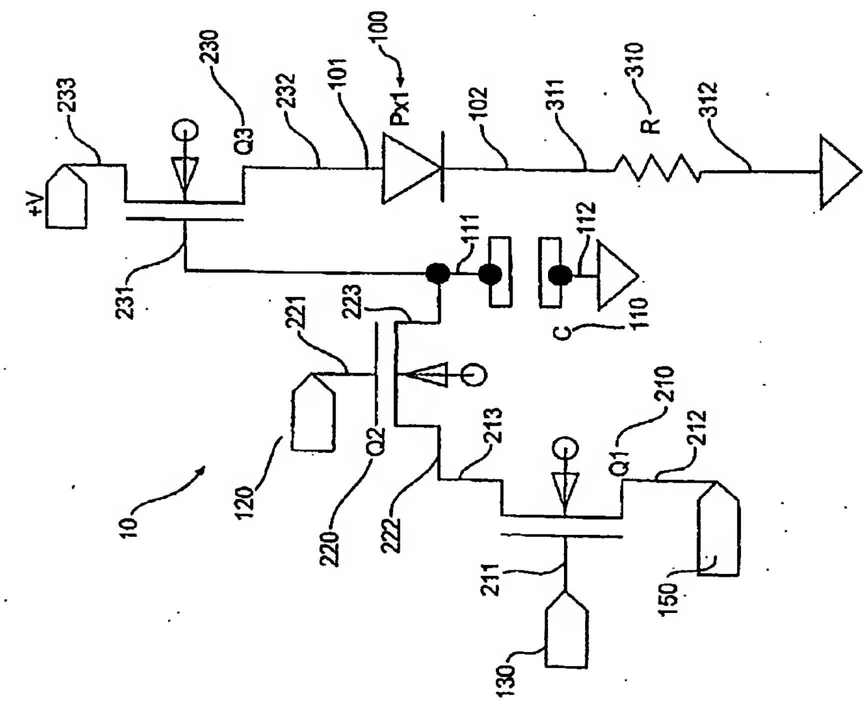

+V
233
230
Q3
232
101
100
Px1
102
311
310
R
312
231
111
112
223
221
C
110
10
120
Q2
220
222
213
Q1
210
212
211
150
130

FIG. 1

2/8

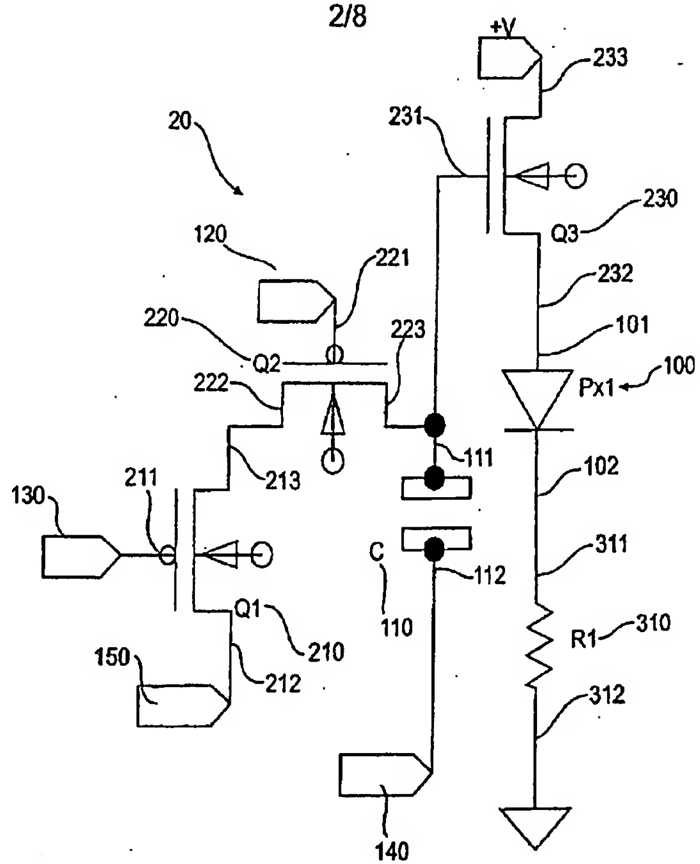


FIG. 2

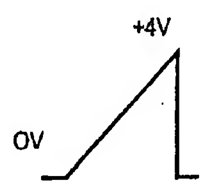


FIG. 2a

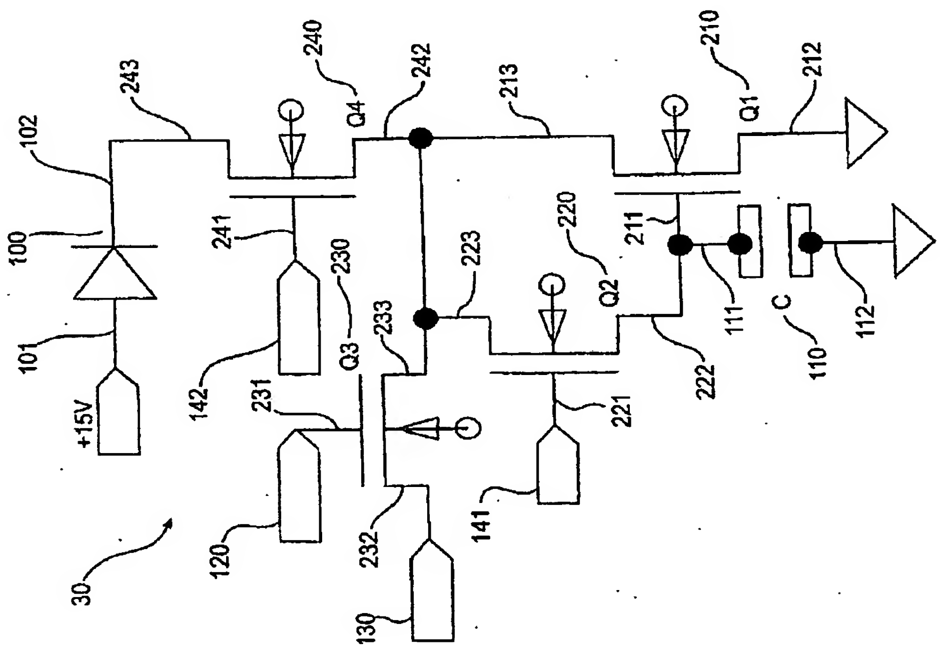
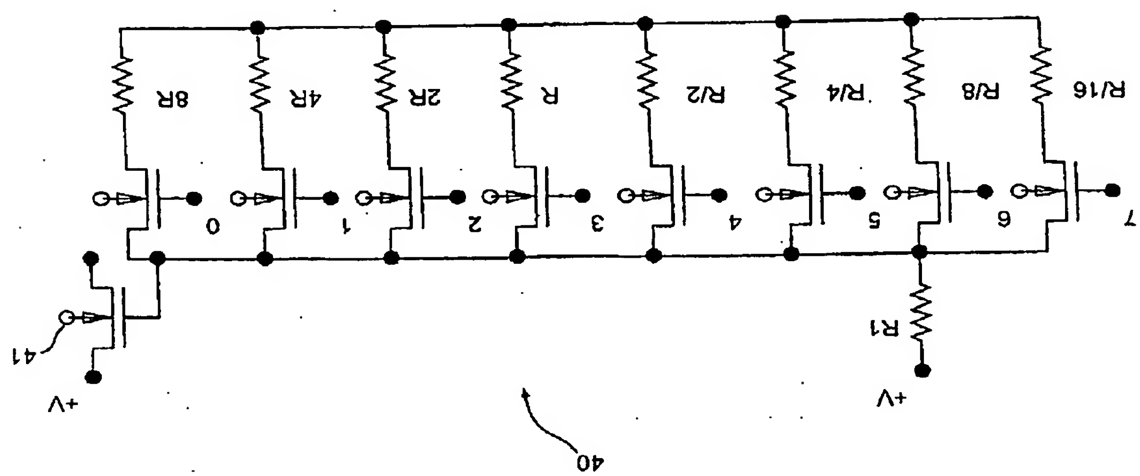

30
+15V
101
100
102
243
240
Q4
242
241
230
142
120
231
Q3
233
232
130
213
223
220
Q2
221
141
222
210
Q1
212
211
111
C
110
112

FIG. 3

FIG. 4



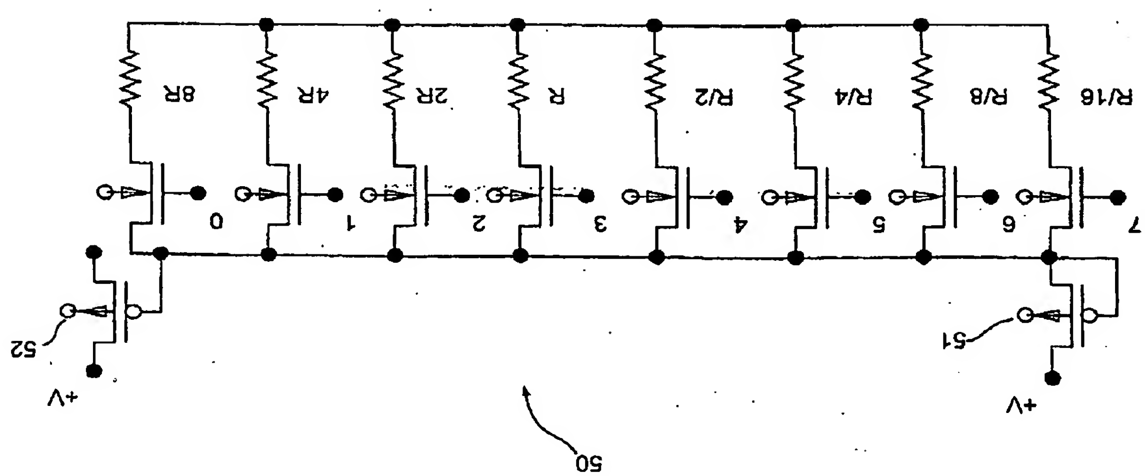
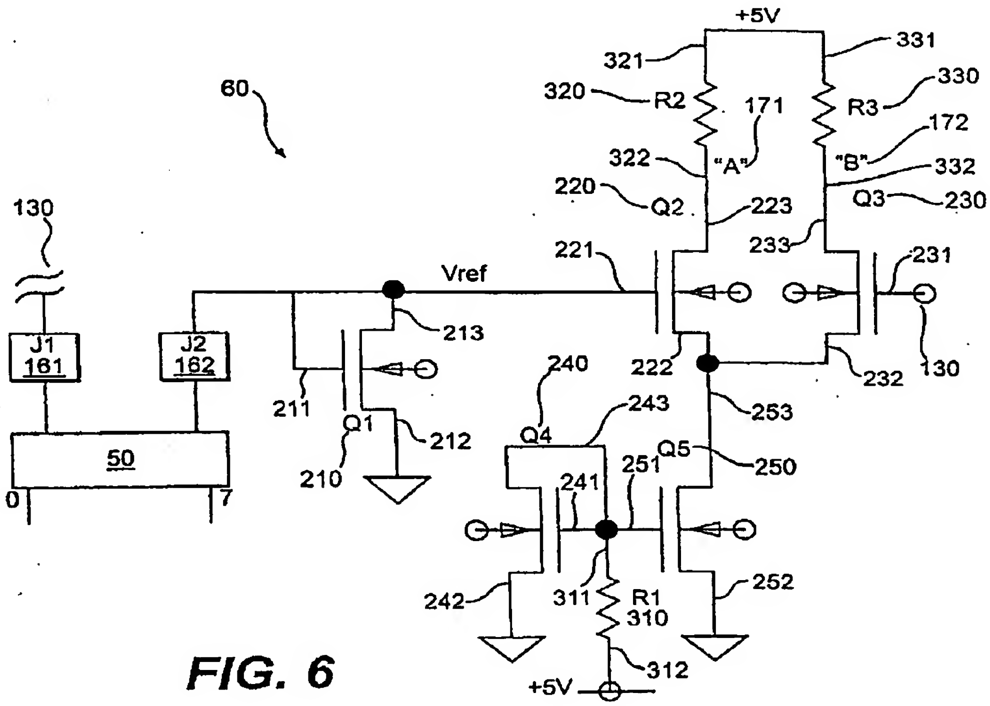


FIG. 5



+5V
321
331
320
R2
171
R3
330
60
322
"A"
"B"
172
332
220
Q2
223
Q3
230
130
221
233
231
Vref
213
J1
161
J2
162
240
222
232
130
211
Q1
243
253
212
Q4
Q5
50
210
241
251
250
0
7
242
311
R1
310
252
312
+5V

FIG. 6

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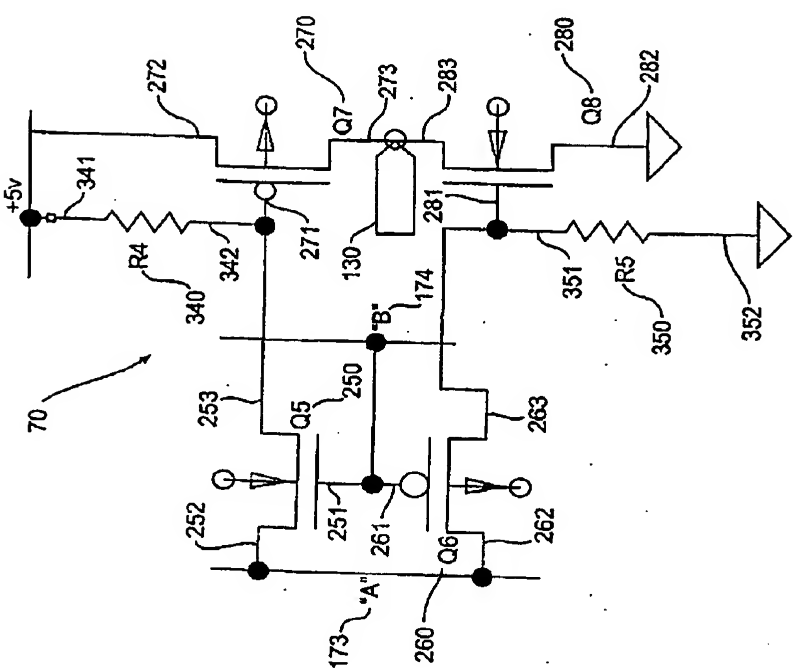
70
+5v
341
R4
340
342
271
272
270
Q7
273
130
283
281
280
Q8
282
351
R5
350
352
"B"
174
253
Q5
250
252
251
261
Q6
262
263
"A"
173
260

FIG. 7

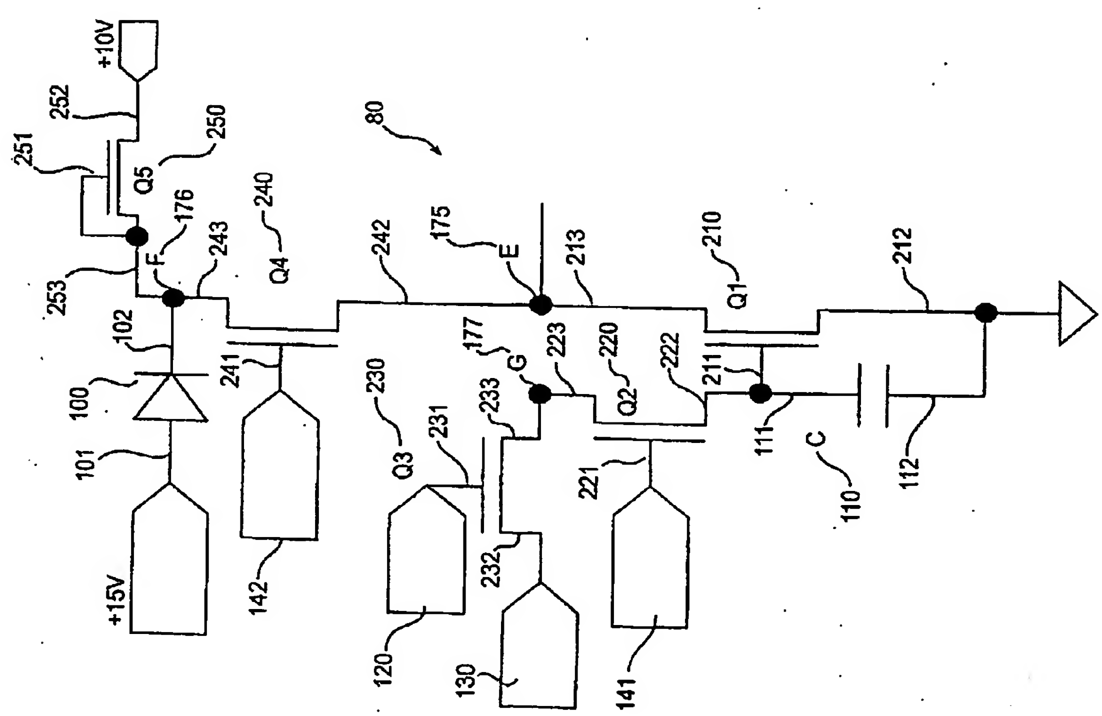
+10V
252
251
Q5
250
253
176
F
243
Q4
240
242
175
E
213
210
Q1
212
102
100
101
+15V
241
142
230
Q3
231
233
177
G
223
220
Q2
222
211
111
C
110
112
221
141
232
120
130

FIG. 8

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US99/01223

A. CLASSIFICATION OF SUBJECT MATTER

IPC(6) : G09G 3/36
US CL : 345/98, 99, 87, 92
According to International Patent Classification (IPC) or to both national classification and IPC.

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

U.S. : 345/98, 99, 100, 208, 87, 89, 90, 92, 55

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

None

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

ACTIVE MATRIX, AM, IMPEDANCE, CURRENT DRIVEN, VOLTAGE DRIVEN, HIGH RESOLUTION, LOW RESOLUTION, PIXEL, PIXEL CIRCUIT, GRAY OR GREY SCALE, HIGH SPEED, LINEAR IMPEDANCE

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 5,017,914 A (UCHIDA ET AL) 21 MAY 1991, see col. 1, lines 9-53; see col. 6, lines 28-42; col. 8, lines 25-28; see col. 1, lines 54-56; col. 2, lines 4-14.	1-13
Y	US 5,589,847 A (LEWIS) 31 December 1996, see figure 15A; col. 5, lines 60-67; see col. 5, lines 54-55; col. 10, lines 49-67; col. 11, lines 1-19; see Figure 14a(C1, C2, Cn); see col. 2, lines 61-67; col. 3, lines 1-5.	1-3, 6, 9-11

☒ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

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Date of the actual completion of the international search 25 FEBRUARY 1999	Date of mailing of the international search report 28 MAY 1999
Name and mailing address of the ISA/US Commissioner of Patents and Trademarks Box PCT Washington, D.C. 20231 Facsimile No. (703) 305-3230	Authorized officer ANTHONY J. BLACKMAN Joni Hill Telephone No. (703) 305-0833

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INTERNATIONAL SEARCH REPORT

International application No.
PCT/US99/01223

C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 5,339,090 A (CROSSLAND ET AL) 16 August 1994, see col. 8, lines 3-37.	12
Y	US 4,872,002 A (STEWART ET AL) 03 October 1989, see col. 1, lines 8-17; see col. 2, lines 53-60.	4-5, 13
Y	US 4,691,200 A (STEPHANY) 01 September 1987, see col. 1, lines 64-68, col. 2, lines 1-14.	7-8

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INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(51) International Patent Classification 6 : G09G 3/36 | A1

(11) International Publication Number: WO 99/38148

(43) International Publication Date: 29 July 1999 (29.07.99)

(21) International Application Number: PCT/US99/01223

(22) International Filing Date: 22 January 1999 (22.01.99)

(30) Priority Data: 60/072,342 23 January 1998 (23.01.98) US

(81) Designated States: US, European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE).

Published
With international search report.
Before the expiration of the time limit for amending the claims and to be republished in the event of the receipt of amendments.

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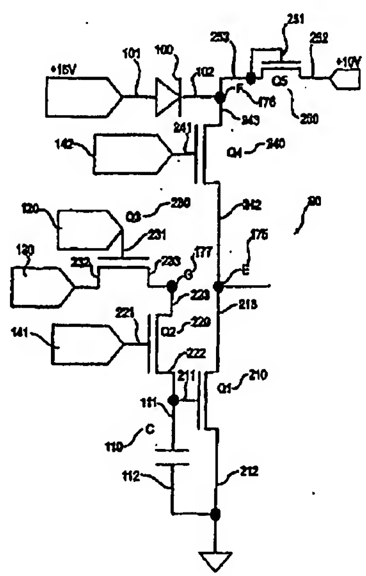
(54) Title: HIGH RESOLUTION ACTIVE MATRIX DISPLAY SYSTEM ON A CHIP WITH HIGH DUTY CYCLE FOR FULL BRIGHTNESS

(57) Abstract

An active matrix display device is disclosed. The display includes individual driver circuits for each pixel (100) to provide accurate, high resolution gray scale rendering and an almost 100 % duty cycle. The pixel circuit drivers (Figures 1(10), 2(20), 3(30), 4(40), 5(50), 6(60), 7(70) and 8(80)) minimize factors known to limit gray scale resolution, such as variations in threshold voltage, voltage drops in connecting lines and from leakage currents, and large peak currents. The present invention includes a line driver functioning initially as a low impedance voltage driver (Figure 6(60)), then converting to a high impedance current driver (Figure 6(60)). A method of driving a pixel (100) with sufficient circuitry to sustain the pixel's light output at a gray level determined by the input data fed to the pixel (100) is also disclosed. The display is capable of processing both digital and analog input data.



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